IN THE CLAIMS

What is claimed is:

1. A voice data processing system, comprising:

at least one status store for storing status information on a plurality of voice channel;

at least one source buffer for storing voice data for the plurality of voice channels; and

a processing system that accesses the at least one status store and generates read addresses for the at least one source buffer to access voice data for only those voice channels having a predetermined status, and generates write addresses for at least one destination buffer for writing the voice data read from the at least one source buffer to at least one destination buffer.

2. The voice data processing system of claim 1, wherein:

the at least one status store includes a valid store for storing at least a valid indication or invalid indication for each voice channels, the valid indication indicating that the corresponding voice channel data is valid, the invalid indication indicating that the corresponding voice channel is not valid; and

the processing system reads voice data from the at least source buffer and writes the voice data to the at least one destination buffer for only those voice channels having a valid indication.

3. The voice data processing system of claim 1, wherein:

the at least one status store includes a silent store that stores at least a silent indication or an active indication for each voice channel, the silent indication indicating the corresponding voice channel is not carrying voice data, the active indication indicating that the corresponding voice channel is carrying voice data; and

the processing system includes an egress engine, the at least one source buffer includes a local buffer coupled to a synchronous data network, and the at least one destination buffer includes a voice packet buffer memory (VPBM) coupled to an asynchronous data network, the egress engine outputting voice data and VPBM addresses for those voice channels when the corresponding silent store indication is active, and does not output voice data and the VPBM address when the corresponding silent store indication is silent.

4. The voice data processing system of claim 3, wherein:

the processing system includes an address generator that generates write addresses from at least a time stamp count value.

5. The voice data processing system of claim 4, wherein:

the VPBM stores voice channel information according to a voice data sample size value, and the write address is generated from more bits of a

timestamp counter for larger sample size values.

6. The voice data processing system of claim 1, wherein:

the status store comprises a dual port memory.

7. The voice data processing system of claim 1, wherein:

the processing system includes a first-in-first-out buffer (FIFO) that stores voice data and corresponding at least one destination buffer addresses for those voice channels having the predetermined status.

8. The voice data processing system of claim 1, wherein:

the processing system includes an ingress engine, the at least one source buffer includes a jitter buffer coupled to an asynchronous data network, and the at least one destination buffer includes a local buffer coupled to a synchronous data network.

9. The voice data processing system of claim 8, wherein:

the processing system includes an address generator that generates write addresses for the local buffer from a status store address.

10. The voice data processing system of claim 8, wherein:

the processing system includes an address generator that generates read addresses for the jitter buffer from at least a time stamp value.

11. The voice data processing system of claim 10, wherein:

the jitter buffer stores voice channel information according to a voice data sample size value; and

the address generator generates read addresses from more bits of a timestamp counter for larger sample size values.

12. The voice data processing system of claim 10, wherein:

the address generator generates read addresses for the jitter buffer from at least a portion of read addresses for the status store.

13. The voice data processing system of claim 12, wherein:

the address generator further generates read addresses for the jitter buffer by adding a base address to an offset address generated from at least a portion of read addresses for the status store and a time stamp count value.

14. The voice data processing system of claim 1, further including:

a data packing circuit that accesses at least one compression status store and packs compressed data into the at least one destination buffer for only those voice channels having a predetermined compression status.

15. The voice data processing system of claim 1, further including:

a data unpacking circuit that accesses at least one uncompression

status store and unpacks uncompressed data into the at least one destination buffer for only those voice channels having a predetermined uncompression status.

16. A voice data processing system, comprising:

at least one local buffer for storing voice data for a plurality of channels that is received from a synchronous voice data source;

at least one voice packet buffer memory (VPBM) for storing voice data for the plurality of channels for transmission over an asynchronous data network;

at least one status store for storing status information for the plurality of voice channels; and

an address generator that accesses the at least one status store for the status information and generates local buffer read addresses and VPBM write addresses for only those voice channels having a first type of status information, the VPBM write addresses being generated from at least one timestamp value.

17. The voice data processing system of claim 16, wherein:

the at least one voice data store includes a first buffer and second buffer, the first local buffer storing voice channel information for a different time period than the second local buffer.

18. The voice data processing system of claim 16, wherein:

the VPBM comprises a plurality of channel entry groups, each channel entry group including 2^x channels, where x is an integer; and

the address generator adds the timestamp value to x bits of the base

address value to generate the VPBM write address.

19. The voice data processing system of claim 16, wherein:

the VPBM comprises a plurality of channel entry groups arranged according to a buffer size value, each channel entry group being addressable by a base address, the address generator increments a first base address by a voice channel number value multiplied by a buffer size value to generate base addresses.

20. A voice data processing system, comprising:

at least one local buffer for storing voice data for a plurality of channels for transmission over a synchronous voice data source;

at least one jitter buffer memory for storing voice data for the plurality of channels that is received from an asynchronous data network;

at least one status store for storing status information for the plurality of voice channels; and

an address generator that accesses the at least one status store for the status information and generates jitter buffer read addresses and local buffer write addresses for only those voice channels having a first type of status information, the jitter buffer write addresses being generated from at least one timestamp value.

21. The voice data processing system of claim 20, wherein:

the at least one status store includes a plurality of addressable entries, each entry including status information for a plurality of voice channels; and

the address generator combines priority decoded status store entry values with a status store address for the status store entry to generate the local buffer write addresses.

22. The voice data processing system of claim 21, wherein:

the at least one jitter buffer includes a first jitter buffer having a first size and a second jitter buffer having a second size; and

the address generator combines group register value with corresponding timestamp values to generate at least a first portion of the jitter buffer read addresses, the timestamp values being masked according to the size of the jitter buffer being read.